AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A gain ~~selector~~ determining stage for ~~selecting~~ determining ~~a gain for a signal processing circuit for amplifying digital audio signals, the stage comprising:~~ a gain signal to be applied to amplify a digital audio signal, the stage comprising:

an input for receiving a parameter of said digital audio signal;

an adjuster for adjusting said parameter dependent on a received volume control signal; and

a gain selector for ~~selecting a gain dependent on said adjusted parameter~~ applying a variable gain function to said volume control signal in order to generate a gain signal for applying to the digital audio signal; and wherein said variable gain function is dependent on said adjusted parameter.

2. (Currently Amended) A ~~selector~~ gain determining stage according to claim 1 wherein the received volume control signal is input to a processor before being passed to the adjuster.

3. (Currently Amended) A ~~selector~~ gain determining stage according to claim 2 wherein the processor comprises a log converter and/or a scaling means.

4. (Currently Amended) A ~~selector~~ gain determining stage according to claim 1 wherein the adjuster comprises a log converter for log converting the received parameter and an adder for adding the volume control signal to the log parameter.

5. (Currently Amended) A ~~selector~~ gain determining stage according to claim 1 wherein the parameter is dependent on the peak value of the received signal.

6. (Currently Amended) A ~~selector~~ gain determining stage according to claim 5 wherein the parameter is a peak level envelope signal.

7. (Currently Amended) A ~~selector~~ gain determining stage according to claim 1 further comprising an input to receive a threshold signal; a comparator for comparing an output of the adjuster with the threshold signal; and wherein the gain selector ~~selects~~ determines the gain dependent on the comparison.

8. (Currently Amended) A ~~selector~~ gain determining stage according to claim 7 wherein the threshold signal is input to a processor before being passed to the comparator.

9. (Currently Amended) A ~~selector~~ gain determining stage according to claim 2 wherein the processor comprises a log converter and/or a scaling means.

10. (Canceled).

11. (Currently Amended) ~~A selector~~ The gain determining stage of claim 7 wherein the gain is ~~selected~~ determined using a variable gain function:

(a) when the output of the adjuster is greater than the threshold signal and a negative signal polarity; or

(b) when the output of the adjuster is less than the threshold signal and a positive signal polarity is utilised.

12. (Currently Amended) The gain ~~selector~~ determining stage of claim 11 ~~10~~ wherein the variable gain function, or a factor of the variable gain, is:

$K = 2^{lgK}$ where

$lgK = lgGs + m(lgGV + lgTA)$

where K is the gain, $lgGs$ is the volume control signal, $lgGV$ is the output of the adjuster, $lgTA$ is the threshold signal and m is a value indicative of a predetermined operational characteristic curve.

13. (Currently Amended) A signal processing circuit for amplifying a digital audio signal, comprising:

parameter determining processor for determining a parameter of said signal;

a gain ~~selector~~ determining stage according to claim 1; and

amplifier for amplifying said signal according to said gain signal.

14. (Original) A circuit according to claim 13 wherein the parameter determining processor is a peak detector.

15. (Original) A circuit according to claim 14 wherein the peak detector output is dependent on the peak levels in the signal waveform and a time dependent decay characteristics, wherein the decay characteristic is further dependent on the frequency of said signal.

16. (Original) A circuit according to claim 15 wherein the peak detector comprises a disabler for disabling the decay characteristic until the signal changes polarity.

17. (Original) A circuit according to claim 13 further comprising a delay for delaying said signal prior to said amplification in order to first determine said gain characteristic.

18. (Currently amended) A circuit according to claim 14 ~~peak detector~~ comprising:

an input for receiving a signal;

peak level processor for determining peak levels in the signal; and

an output for outputting a signal dependent on said peak levels and a time dependent decay characteristic, wherein the decay characteristic is further dependent on the frequency of said received signal.

19. (Currently amended) A detector according to claim 18 ~~13~~ wherein the output comprises a disabler for disabling the decay characteristic until the signal changes polarity.

20. (Currently amended) A circuit according to claim 14 ~~signal level detector~~ comprising:

an input to receive an input audio signal;

an amplitude processor operable in a decay mode, being when the input audio signal is smaller than a previous output signal, whereby in the decay mode, the processor is configured to generate a signal for decreasing the amplitude of a signal to be output; and

a logic device for controlling the operation of the amplitude processor in the decay mode such that the processor only generates a signal in the decay mode upon receipt of a trigger from the logic device, whereby the trigger is related to the frequency of the input audio signal.

21. (Currently amended) A circuit according to claim 14 ~~signal level detector~~ comprising:

an input to receive in input audio signal;

an amplitude processor configured to generate a signal for scaling the amplitude of a signal to be output; and

a logic device for controlling the operation of the amplitude processor such that the processor only generates the signal for scaling upon receipt of a trigger from the logic device, whereby the trigger is related to the frequency of the input audio signal.

22. (Original) The signal level detector of claim 20 further comprising a comparator for determining when a change for sign occurs, wherein the comparator is associated with the logic device, and the logic device sends a trigger to the amplitude processor when a change of sign of the input signal occurs.

23. (Original) The signal level detector of claim 20 wherein the logic device comprises an input for receiving a timeout signal, and the logic device sends a trigger to the processor when a timeout signal is received.

24. (Original) The signal level detector of claim 23 further comprising a timeout counter which is configured to generate the timeout signal after a time period passes, corresponding to the lowest frequency of the input signal, without a change of sign occurring.

25. (Amended) A method according to claim 38 wherein determining the peak level envelope comprises ~~of determining a signal level of an audio signal comprising~~:

receiving an input audio signal;

comparing the input audio signal with a previous output signal to obtain a difference signal;

generating a scaled signal by scaling the difference signal using an attack coefficient or a decay coefficient, depending upon the comparison;

combining the scaled signal with the previous output signal to obtain a signal, indicative of the signal level of the input audio signal, characterised in that the method comprises:

controlling the generation of the scaled signal when scaled by the decay parameter, using a trigger related to the frequency of the input audio signal.

26. (Original) The method of claim 25 wherein only the generation of the indicative signal scaled signal by a decay parameter is controlled.

27. (Original) The method of claim 25, wherein the trigger is generated when a change of sign of the input signal occurs or a timeout occurs.

28. (Canceled).

29. (Currently amended) An integrated circuit comprising a circuit ~~gain selector stage~~ according to claim 13 [[1]].

30. (Currently amended) Audio equipment comprising an integrated ~~integrator~~ circuit according to claim 29 ~~28~~.

31. (Canceled).

32. (Currently amended) Processor control code to, when, running, implement the signal processing ~~circuit~~ method of claim 37 ~~13~~.

33. (Currently amended) A carrier carrying the processor control code of claim 32 ~~31~~.

34. (Currently amended) The circuit ~~signal level detector~~ of claim 21, further comprising a comparator for determining when a change of sign occurs, wherein the comparator is associated with the logic device, and the logic device sends a trigger to the amplitude processor when a change of sign of the input signal occurs.

35. (Currently amended) The circuit ~~signal level detector~~ of claim 21 wherein the logic device comprises an input for receiving a timeout signal, and the logic device sends a trigger to the processor when a timeout signal is received.

36. (Original) The signal level detector of claim 35, further comprising a timeout counter which is configured to generate the timeout signal after a period of time passes, corresponding to the lowest frequency of the input signal, without a change of sign occurring.

37. (New) A method of determining a gain signal for applying to a digital audio signal; the method comprising:

receiving a parameter of said digital audio signal; adjusting said parameter dependent on a received volume control signal; applying a variable gain function to said volume control signal in order to generate the gain signal for applying to the digital audio signal, and wherein said variable gain function is dependent on said adjusting parameter.

38. (New) The method of claim 37 wherein the parameter is the peak level envelope signal of the digital audio signal.

39. (New) A method of amplifying a digital audio signal, comprising:

determining a parameter of said signal;

determining a gain signal according to claim 24; and

amplifying said digital audio signal by applying said gain signal.